Gigabit Video Interface : A Fully Serialized Data Transmission System for Digital Moving Pictures

Hidekazu Kikuchi, Tatsuya Fukuzaki, Ryo Tamaki, Tohru Takeshita

Mixed Signal Department, Semiconductor Company, SONY corporation
4-14-1 Asahi-cho, Atsugi-shi, Kanagawa-ken, 243 JAPAN
kikuchi@sabip.semicon.sony.co.jp

Abstract

A 1-bit serial 1.56Gb/s data transceiver chip set for base band transmission of XGA moving pictures was developed. It integrates PLLs, ENC/ DEC, cable driver/equalizer and synchronization controllers required for transmission without any expensive external devices.

1. Introduction

High resolution LCD monitors and projectors for PCs and other multimedia systems are emerging and picture data for LCD are transmitted in mainly analog signal today, but analog transmission has drawbacks in both picture quality and transmission length. Digital transmission was achieved by serial bus (IEEE1394) [1]with data compaction or semi-serialized base band transmission (VESA P&D)[2] as shown in Figure 1, but the 1394 with compaction requires significant amount of hardware overhead, while for the semi-serialized transmission, too many twisted pairs must be used. A moving picture transmission system with much simpler hardware and thinner and longer cable drive capability is desired for forthcoming multimedia systems.
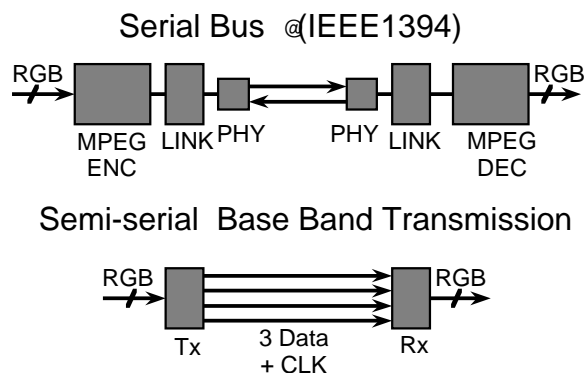
The block diagram of the proposed Gigabit Video Interface (GVIF) is shown in Figure 2. It's a 1-bit serial data transmission system using a 1.56Gb/s PLL-based serializer/deserializer (SER/DES) technique. The existing high-speed SER/DES, such as 1.06Gb/s Fibre Channel, 1.25Gb/s Ethernet and 1.48Gb/s SDI, need external encoder/decoders (ENDEC), controllers, reference clock sources, and E/O, O/E devices or cable equalizers for transmission, which make total cost of transmission expensive. The GVIF employs a simple ENDEC and a self-control system and the total system is integrated into 1-chip transmitter and 1-chip receiver. The receiver LSI also integrates a cable equalizer which makes it possible to transmit XGA moving pictures via only one differential cable of 5 mm diameter over 20m length, without using optical fibers or special cables.
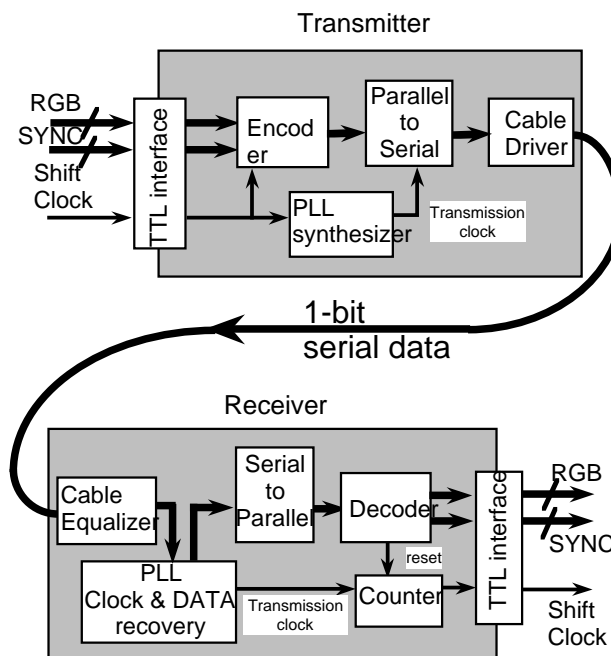

Figure 1: Conventional Schemes for the moving picture transmission

Figure 2: Block diagram of proposed transceiver chip set

2. Coding technique

A newly developed ENDEC in the GVIF is based on 3B4B encoding. The encoder translates 18-bit RGB data and 6-bit SYNC/CNTL signals into a 24-bit word for serial NRZ data transmission, as shown in Figure 3. It is designed to keep DC balance well and to keep data transmission density high in serial data stream to assure stable operation of clock & data recovery (CDR) in the receiver LSI.

3. Self-controlled lock-in system

As shown in Figure 4, the GVIF also employs a self-control system for the CDR to lock-in to serial data without any help of off-chip controllers or reference clocks. The GVIF uses a common mode voltage of the differential cable as acknowledge of CDR status and the transmitter sends reference signal temporarily to help the receiver to lock-in. The GVIF achieved hot-plug capability without external reference clock source for the CDR by this self control.

4. Cable equalizer

Another feature of the GVIF is an integrated cable equalizer in the receiver LSI. It automatically compensates sqrt(f)dB attenuation of the cable.[3] A high speed signal amplitude detector (Figure 5) was newly developed to control the compensation circuit. The GVIF shows stable picture transmission over 20m differential cable though it uses a low voltage swing of 400mv(p-p) in order to keep EMI at a low level.

5. Experimental results

The proposed GVIF transceiver chip set were fabricated in the 0.8um double-polySi Bipolar technology and packaged in the plastic QFP. They transmitted XGA moving picture up to 20m via only one pair of twisted pair cable of φ=4.5mm. The maximum dot clock was 74MHz. The chip set performance is summarized in Table 1.

Dot cycle in which synchronous/control signals are static

18bit RGB data

Transition rich & well DC balanced 24bit code
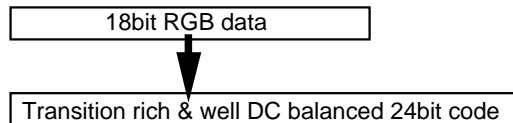
Dot cycle in which synchronous/control signals transit

18bit RGB data

6bit Header | 18bit RGB data

Figure 3: Architecture of 18B24B coding

6. Conclusion

The GVIF is designed to reduce the total cost of digital moving picture data transmission by eliminating external devices and using minimum pin count of cable and connectors, and it provides unique features of long cable drivability and space saving connection.

References
[1] IEEE-1394-1995 Standard, 1995
[2] VESA Plug and Display Standard, 1997
[3] A.J.Baker;"An Adaptive Cable Equalizer for Serial Digital Video Rate to 400Mb/s", *ISSCC Dig. Tech. Papers,pp174-175,1996*
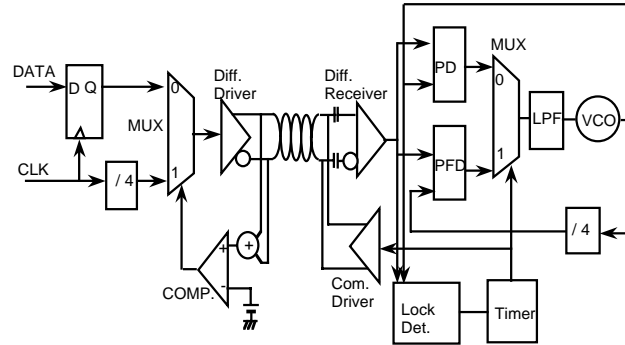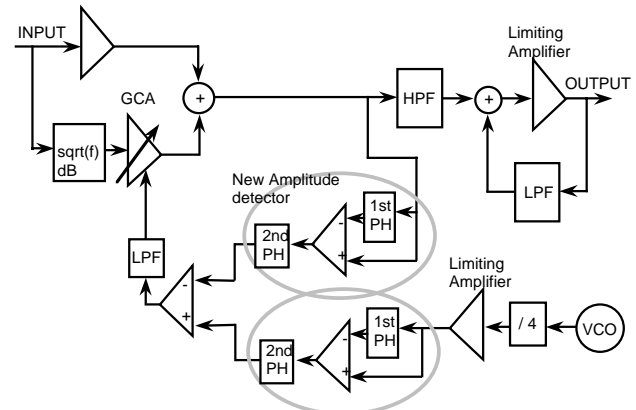
Figure 4: CDR self controlled lock-in system

Figure 5: High-speed cable equalizer with new amplitude detector

Table 1: Performance of transceiver chip set

Technology	0.8um Double-polySi Bipolar process
Chip size	4.2 x 4.2mm.sq(Tx) 4.2 x 4.2mm.sq(Rx)
Chip Power	0.8W typ.(Tx) 1.0W typ.(Rx)
Bit Rate	1780Mb/s @max.