Gigabit Video Interface

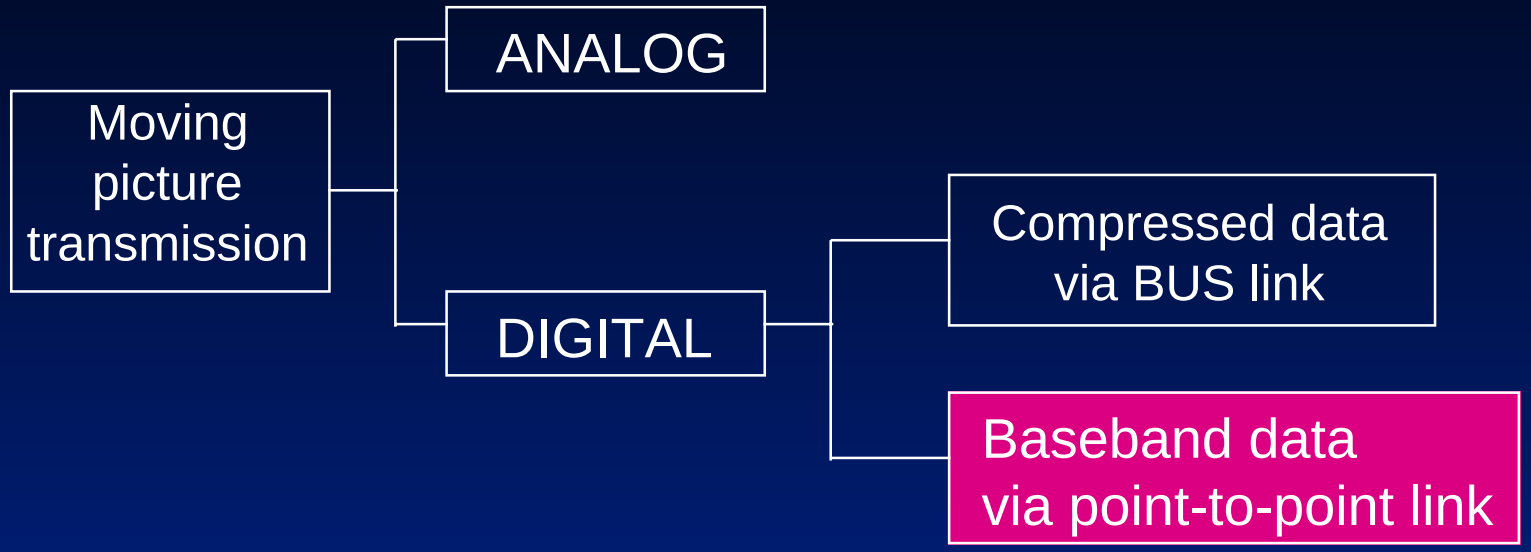
A Fully Serialized Data Transmission System for Digital Moving Picture

Hidekazu Kikuchi, Tatsuya Fukuzaki, Ryo Tamaki
& Tohru Takeshita
Mixed Signal Department, Semiconductor Company, SONY corporation
4-14-1 Asahi-cho, Atsugi-shi, Kanagawa-ken, 243 JAPAN
kikuchi@sabip.semicon.sony.co.jp

OUTLINE

- Background
- Basic concept
- Problems to be solved
- Key technologies
- Results from experiments
- Conclusions

Transmission architectures



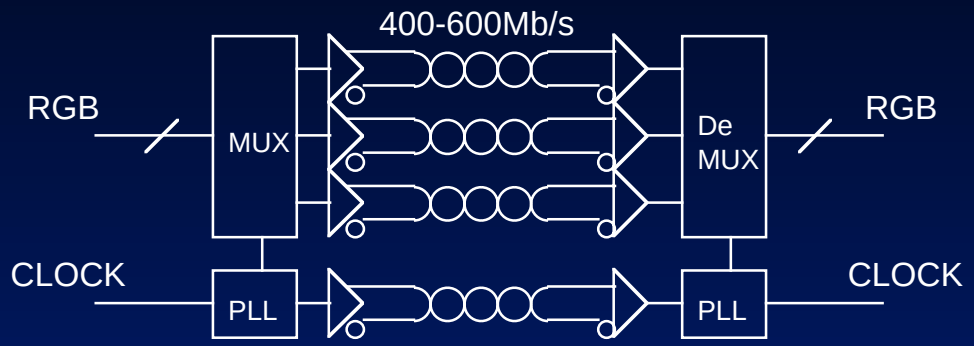
- Baseband transmission is suitable for PC monitor interface

Requirements for the digital monitor IF

- Small connector & thin cable
- Long cable
- Simple hardware

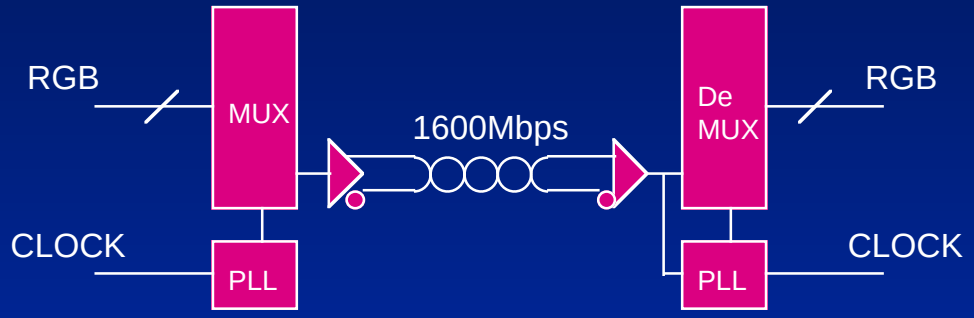
Basic concept

Conventional baseband transmission



Several pairs of differential signal

- Gigabit Video Interface proposal

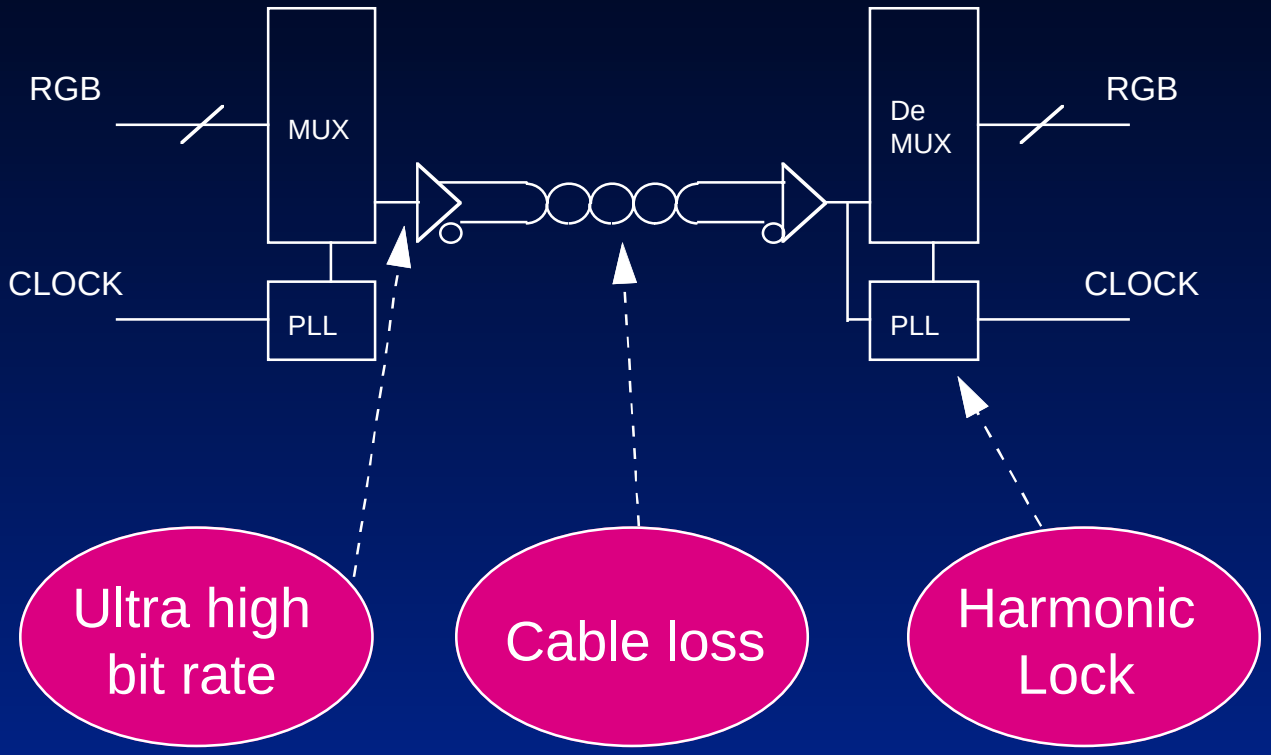


Only 1 pair of differential signal

- Small connector
- Thin cable
- Skew free

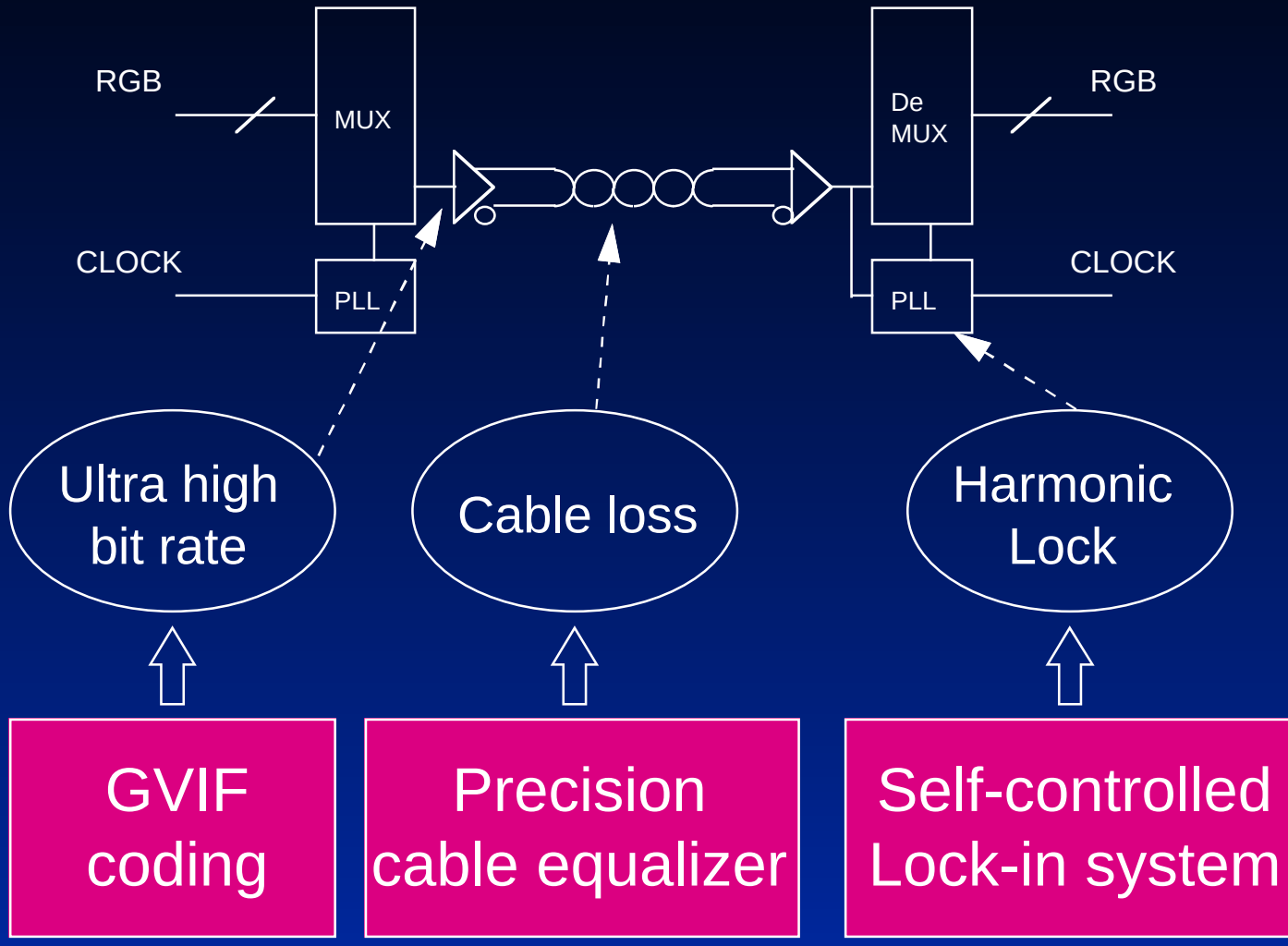
= long drive

Problems to be solved



by simple hardware

Key technologies

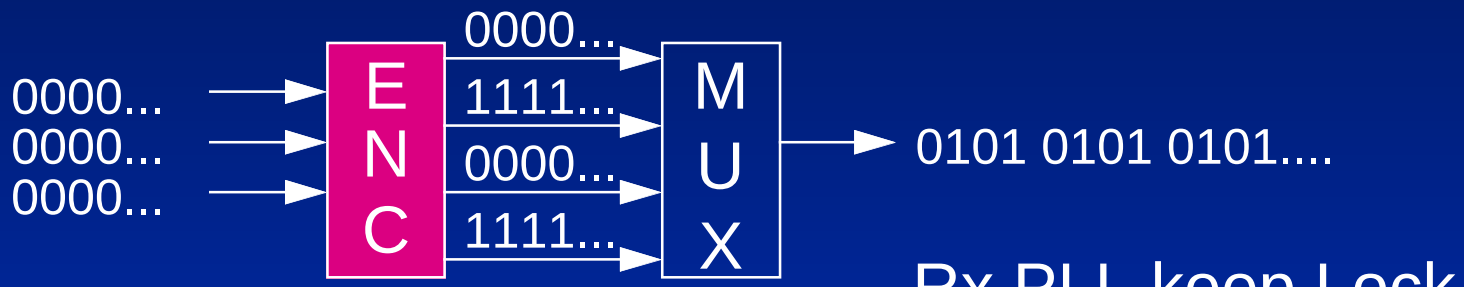


Objective of coding

- Direct Data Multiplex

Rx PLL lose LOCK

- Encoded Data Multiplex



Rx PLL keep Lock

Bits increment by coding

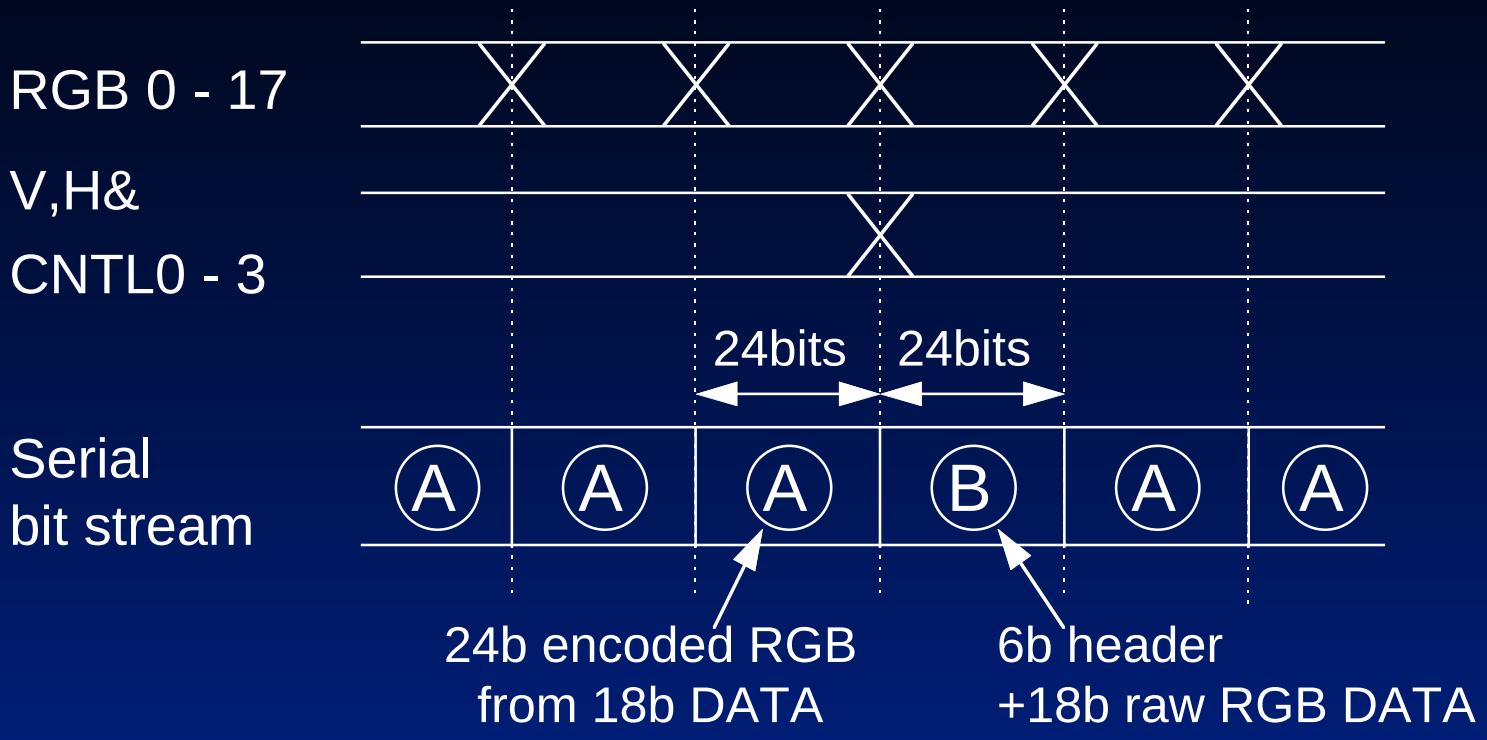
Raw Data — Encoded Data

Total 22 - 24bits —conventional coding→ 28 - 30bits

18bits	RGB
2bits	H/V
1bit	DE(blank*)
1 - 3bits	CNTL(back light, etc)

NEW CODING have to
- *reduce bits* of CODE.
- be realized in *small hardware.*

GVIF coding



- **Efficient code**

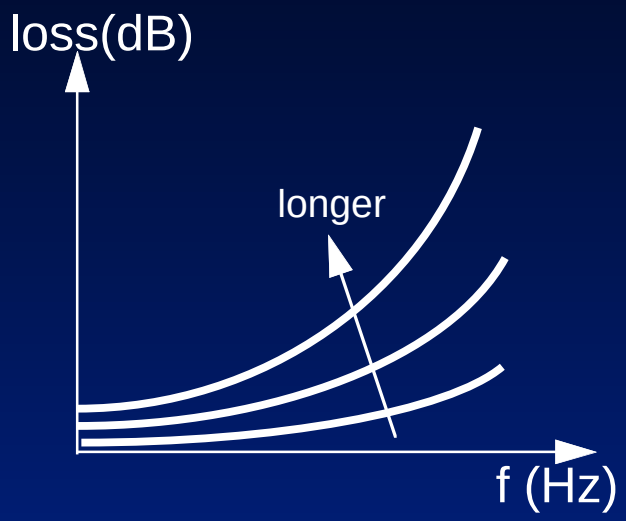
  RGB 18bits + CNTL 6bits ⟶ 24bits CODE

- **Small hardware**

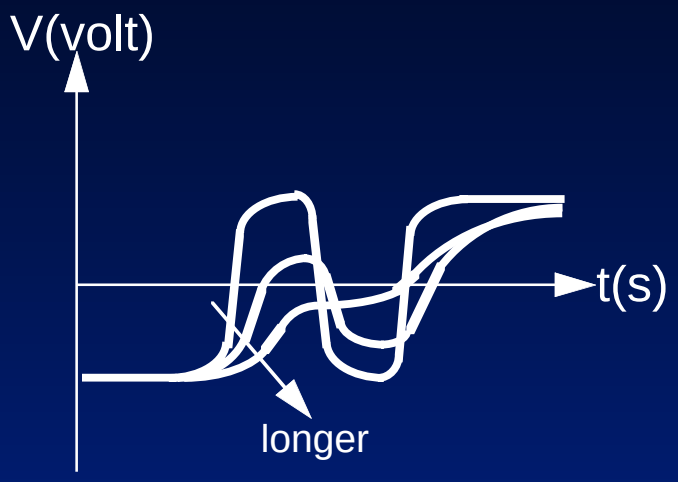
  ENC 250Gates / DEC 250Gates

Cable loss

Frequency domain

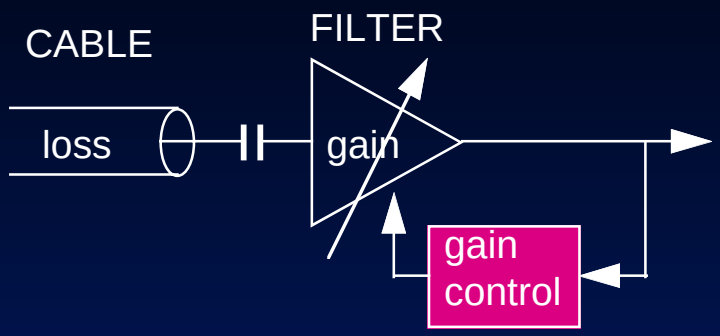


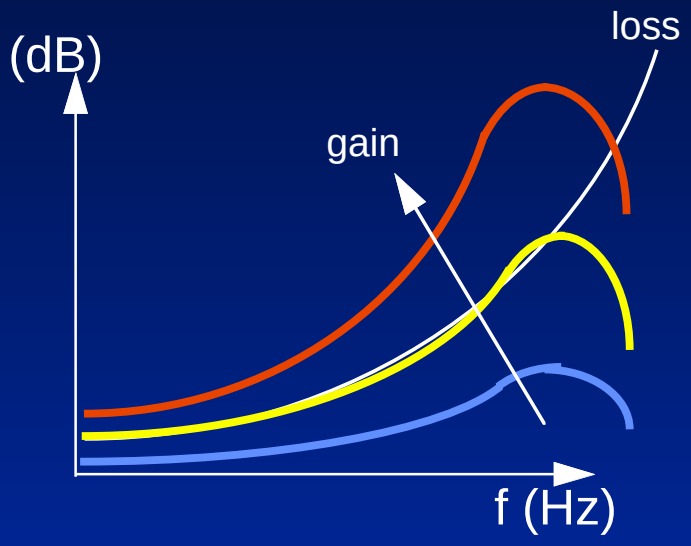
Time domain

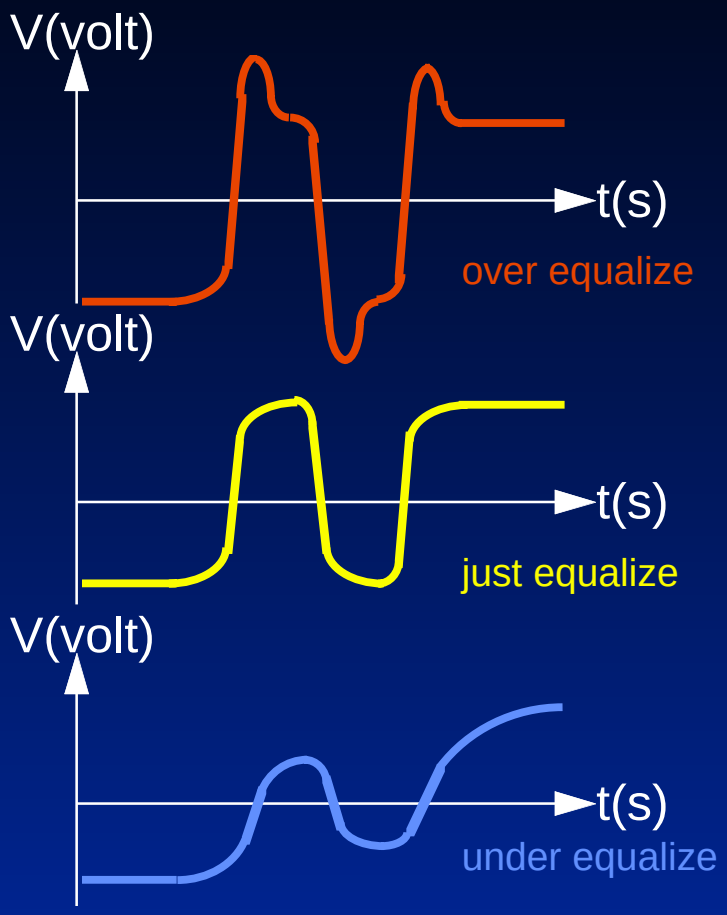


- High speed 1bit transmission requires **Cable Equalizer**

Adoptive cable equalizer



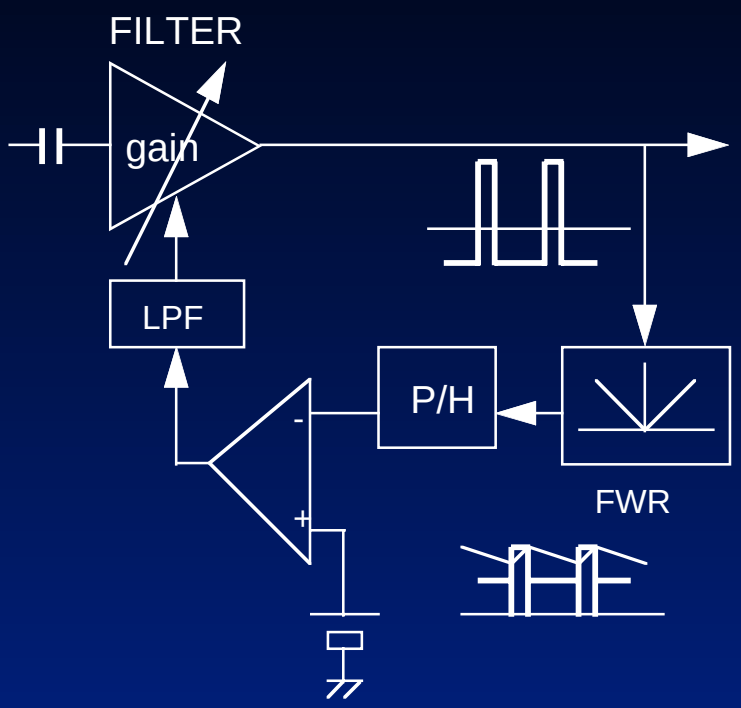




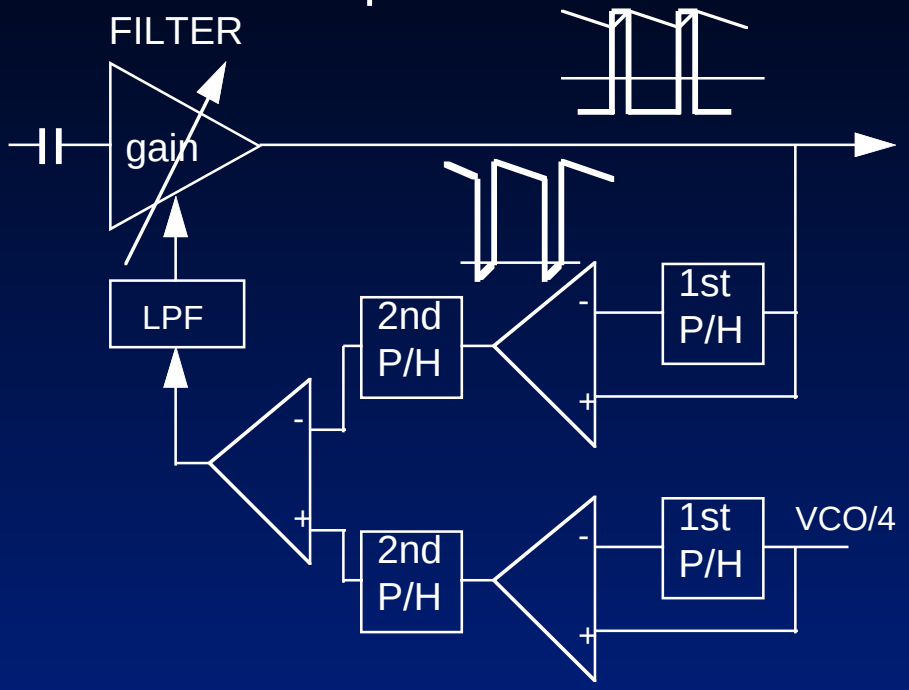
- **Precision gain control** is required

Gain controller for equalizer

Conventional



Proposal



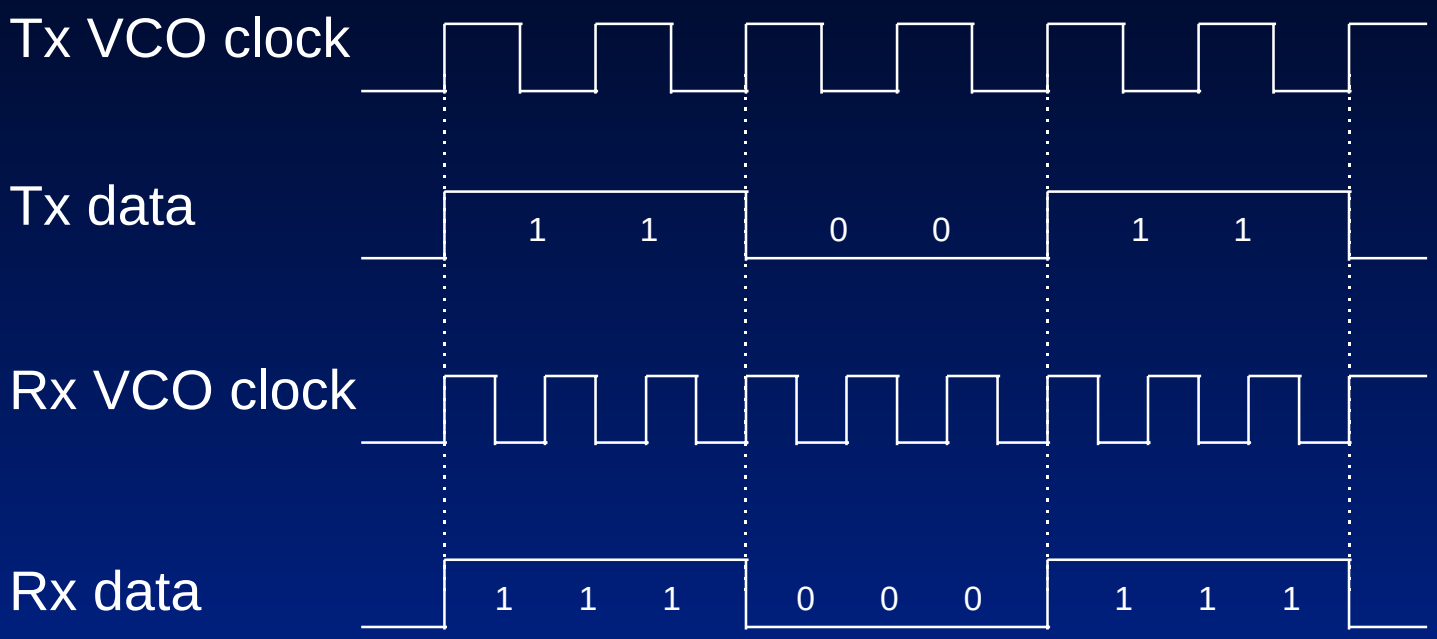
Problems:

- FWR error by duty change
- P/H error by short pulse

Introduced:

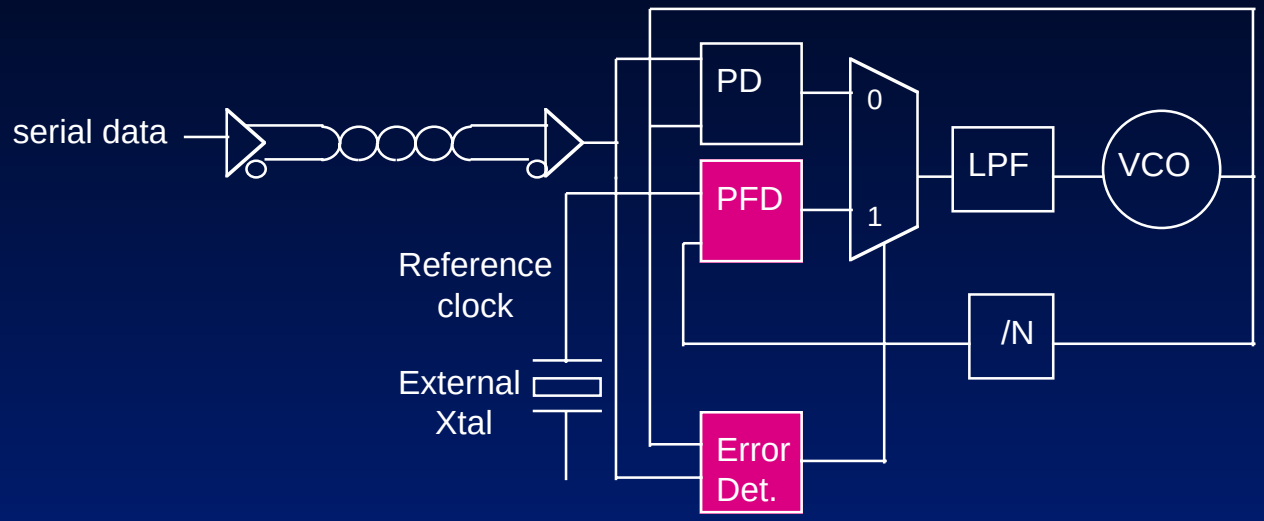
- **2 steps P/H**
- **Active reference**

Harmonic lock in Rx PLL



Conventional lock-in system

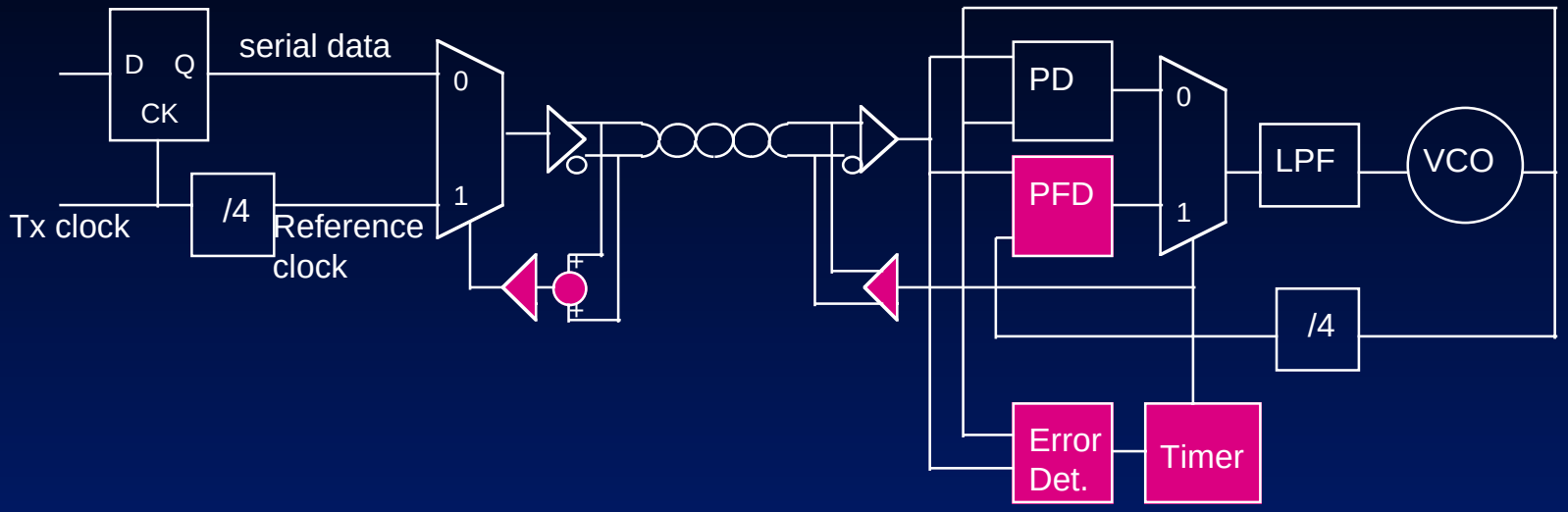
•Use external reference clock



•Use narrow band VCO or filter

Only available for fixed transmission rate

Self-controlled lock-in system



- Serial data / reference clock

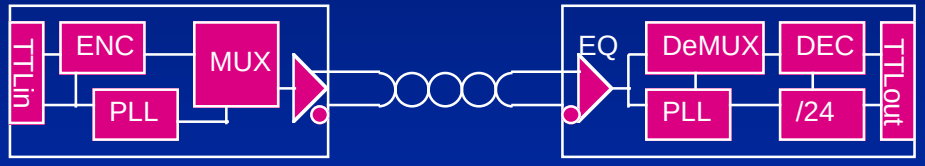
  Tx to Rx in differential mode

- Reference clock request

  Rx to Tx in common mode

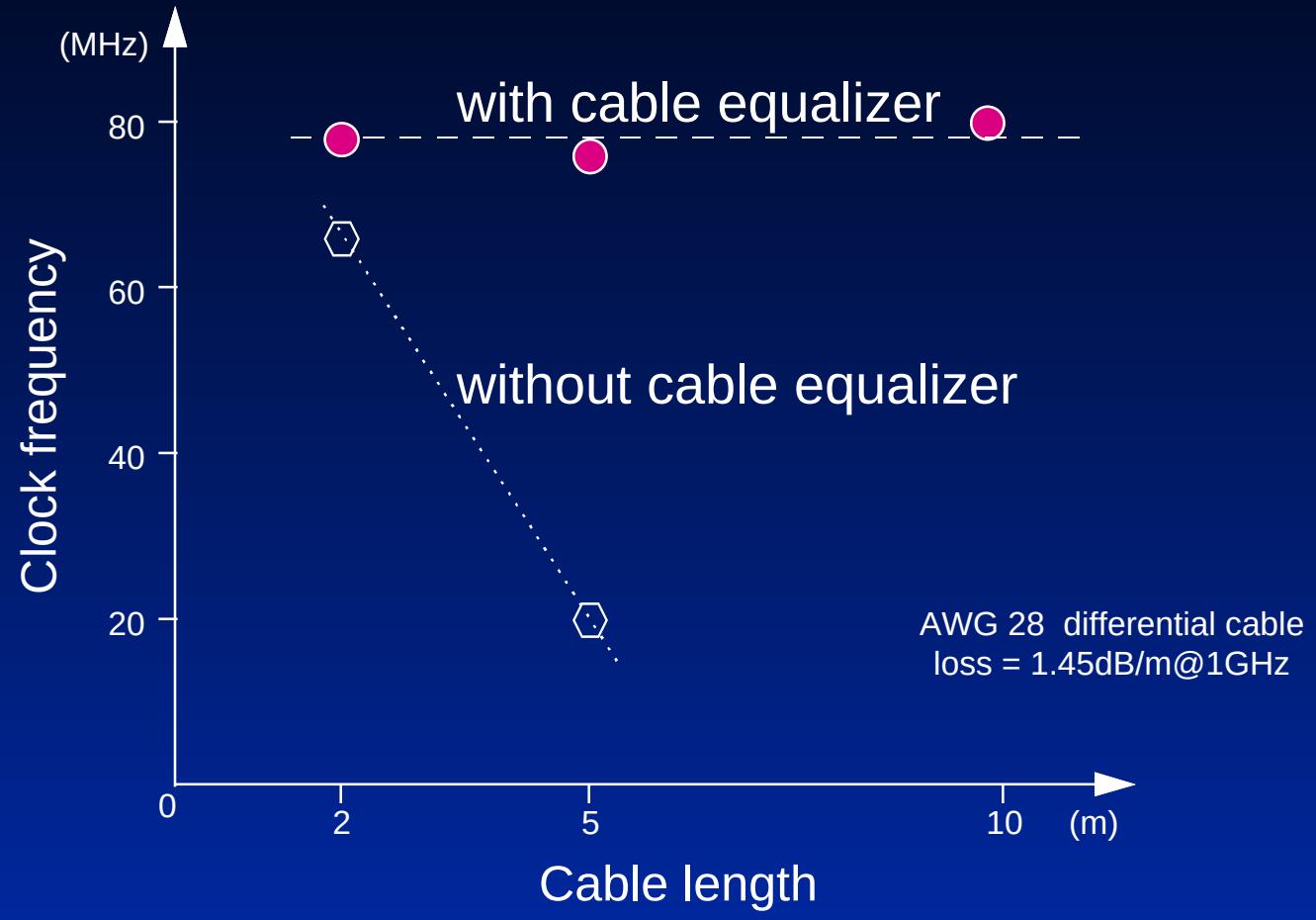
Test chipset

	Tx	Rx
function	18bits RGB +2bits SYNC +4bits Control transmission	
technology	0.8μm Double - poly Si Bipolar Process	
chip size	4.2mm x 4.2mm	4.2mm x 4.2mm
device count	8,900	12,000
chip power	0.8w	1.0w
clock freq.	20 – 74 MHz	
bit rate	480 – 1776 Mb/s	



Experimental results

maximum transmission rate



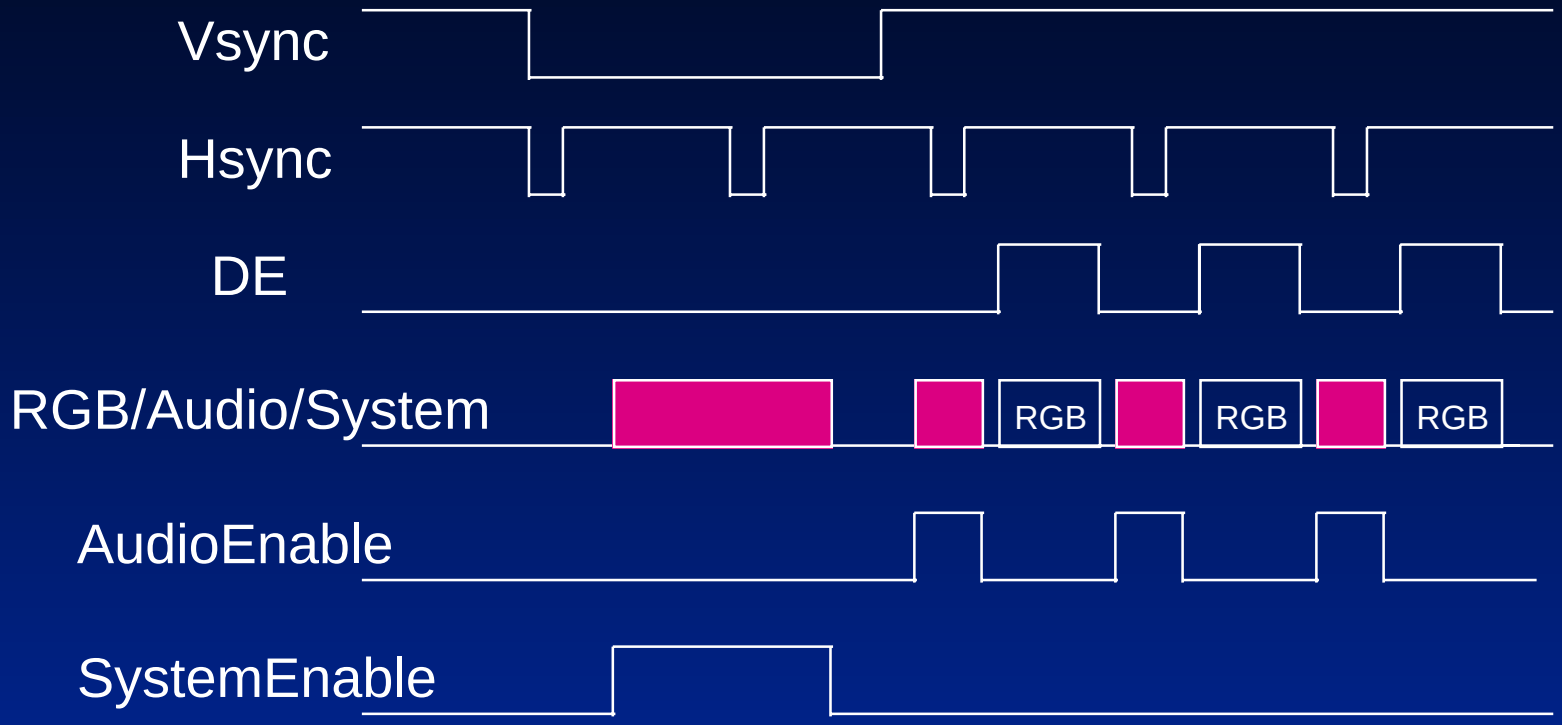
CONCLUSIONS

Gigabit video interface architecture realized XGA moving picture transmission

- via single differential cable
- over 10m
- using only 21K integrated devices

GVIF coding

- **Suitable for packing payload into blank time**



because it always carries 18bits data